WHAT IS CLAIMED IS:

1. A current mirror circuit comprising a current mirror section which includes (A) an input-side transistor whose collector is connected to a signal source and (B) an output-side transistor whose base and collector are connected with each other in a diode structure, said current mirror circuit further comprising:

an adjusting transistor having (i) an emitter connected to the collector of said output-side transistor and (ii) a base connected to the collector of said input-side transistor,

said adjusting transistor having an area of an epitaxial layer which is equal to a product of a reciprocal of a current ratio of said current mirror section and a sum of areas of epitaxial layers in said input-side transistor and said output-side transistor.

2. The current mirror circuit as set forth in claim 1, further comprising:

a voltage equilibrating transistor located between said signal source and said input-side transistor, said voltage equilibrating transistor having (i) an emitter connected to the collector of said input-side transistor, (ii) a base connected to the base of said adjusting transistor, and (iii) a collector connected to said signal source, said

base and said collector of said voltage equilibrating transistor being connected with each other,

a sum of areas of epitaxial layers in said voltage equilibrating transistor and said adjusting transistor being a product of a reciprocal of a current ratio of said current mirror section and a sum of areas of epitaxial layers in said input-side transistor and said output-side transistor.

3. The current mirror circuit as set forth in claim 1, wherein:

said input-side transistor, said output-side transistor, and said adjusting transistor are p-type transistors,

emitters of said input-side transistor and said output-side transistor are both connected to a high-level power supply, and

a collector of said adjusting transistor outputs an output current.

4. The current mirror circuit as set forth in claim 1, wherein:

said input-side transistor, said output-side transistor, and said adjusting transistor are n-type transistors,

emitters of said input-side transistor and said output-side transistor are both connected to a low-level power supply, and

a collector of said adjusting transistor absorbs an output current.

5. The current mirror circuit as set forth in claim 1, wherein:

said adjusting transistor has a parallel-element structure or a multi-collector structure.

6. An optical signal circuit comprising the current mirror circuit as set forth in claim 1.

7. A current mirror circuit provided in an integrated circuit, wherein:

an area of an epitaxial layer is adjusted in accordance with a current ratio of the current mirror so as to eliminate an influence of a photocurrent due to a parasitic photodiode.

8. The current mirror circuit as set forth in claim 7, comprising:

a pair of an input-side transistor Q1 and an output-side transistor Q2, which constitute a current

mirror section, each having an emitter connected to a high-level power supply; and

an adjusting transistor Q3 having (i) an emitter supplied with a collector current of said output-side transistor Q2 whose base and collector are connected with each other in a diode structure, (ii) a base connected to a collector of said input-side transistor Q1, and (iii) a collector that outputs an output current,

a signal source 42 drawing out a current from the collector of said input-side transistor Q1,

each of said transistors Q1, Q2, and Q3 being a p-type transistor in which an n-type epitaxial layer is formed on a p-type substrate layer,

S3 satisfying $S3 = (I1/I2) \times (S1 + S2)$, where S1, S2, and S3 are areas of the n-type epitaxial layers in said transistors Q1, Q2, and Q3, respectively, and I2/I1 is a current ratio of said current mirror section.

9. The current mirror circuit as set forth in claim 8, further comprising:

a voltage equilibrating transistor Q4 located between said signal source 42 and said input-side transistor Q1,

said voltage equilibrating transistor Q4 including:

(i) an emitter connected to the collector of said input-side transistor Q1; and

(ii) a base and a collector connected with each other, and connected to said signal source 42 and the base of said adjusting transistor Q3,

said voltage equilibrating transistor Q4 being composed of a p-type transistor,

an area S4 of an n-type epitaxial layer in said voltage equilibrating transistor Q4 satisfying S3 + S4 = (I1/I2) × (S1 + S2).

10. The current mirror circuit as set forth in claim 7, comprising:

a pair of an input-side transistor Q11 and an output-side transistor Q12, which constitute a current mirror section, each having an emitter connected to a low-level power supply; and

an adjusting transistor Q13 having (i) an emitter supplied with a collector current of said output-side transistor Q12 whose base and collector are connected with each other in a diode structure, (ii) a base connected to a collector of said input-side transistor Q11, and (iii) a collector that absorbs an output current,

a signal source 42 outputting a current into the collector of said input-side transistor Q11,

each of said transistors Q11, Q12, and Q13 being an n-type transistor in which an n-type epitaxial layer is

formed on a p-type substrate layer,

S13 satisfying S11 = (I11/I12) × (S12 + S13), where S11, S12, and S13 are areas of the n-type epitaxial layers in said transistors Q11, Q12, and Q13, respectively, and I12/I11 is a current ratio of said current mirror section.

11. The current mirror circuit as set forth in claim 10, further comprising:

a voltage equilibrating transistor Q14 located between said signal source 42 and said input-side transistor Q11,

said voltage equilibrating transistor Q14 including:

(i) an emitter connected to the collector of said input-side transistor Q11; and

(ii) a base and a collector connected with each other, and connected to said signal source 42 and the base of said adjusting transistor Q13,

said voltage equilibrating transistor Q14 being composed of an n-type transistor,

an area S14 of an n-type epitaxial layer in said voltage equilibrating transistor Q14 satisfying S11 + S14 = (I11/I12) × (S12 + S13).

12. The current mirror circuit as set forth in claim 8, wherein:

said adjusting transistor Q3 has a parallel-element structure or a multi-collector structure.

13. The current mirror circuit as set forth in claim 10, wherein:

said adjusting transistor Q13 has a parallel-element structure or a multi-collector structure.

14. An optical signal circuit using the current mirror circuit as set forth in claim 7.